Internship Ideas

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The offered positions fall into one of the following scientific fields: FPGA prototyping, VHDL/VERILOG programming, computer architecture, computer arithmetic, compilers (LLVM), OS drivers (Android,) graphics algorithms και Neural Network applications.

1. LLVM Compiler Backend and Frontend for GPUs

LLVM is the main compiler tool used in the company. The purpose of this task is to further optimize the backend or front-end parts of LLVM and perform various optimizations, benchmarking, and verification activities. The underlying architecture will be based on Nema GPU, the new programmable, multicore GPU of the company.
Skills required: compiler background, computer architecture, basic knowledge of compiler optimizations.

2. VLSI-level Power Simulator for Nema GPU

One of the current activities of the company is to build a highly accurate power model for the current and under development GPUs. In this task, you will be requested to build a performance monitoring architecture and to gain experience in the lasted power simulation/improvement tools of Cadence.
Skills required: good knowledge HDL/Verilog, background in power reduction theory.

3. Evaluation of Neural and Deep Learning Algorithm in Nema GPUs

The target is to evaluate and extract specific types of parallelization (data-level, thread level, and task-level) in specific applications from the Neural and Deep Learning domain. The target applications will be based in well-known Neural Network frameworks and will be ported in Nema GPUs.
Skills required: good programming skills, parallel architectures.

4. Extend the SystemC-based emulator of Think Silicon to support new features

SystemC is a powerful library facilitating the simulation of computing systems at various abstraction levels. In this project, you are requested to enhance the internal simulator of Think Silicon with new features supporting the execution of OpenCL or OpenGL applications.
Skills required: good programming skills, computer architecture, logic design.

5. Implementation of ASTC Compression/Decompression Algorithm

ASTC is the latest texture compression algorithm developed by ARM (used in Mali GPU). ASTC is expected to be included in the upcoming OpenGL standards. In this task, you are requested to implement (part or all) of the (de-)compression algorithm in Verilog HDL and also in the internal software emulator of the company.
Skills required: Verilog/VHDL programming, logic design, computer architecture.

6. Extending the OpenGL/Vulkan API Implementation with new Features

The company is developing an end-to-end graphics library and driver to accelerate graphics applications written in OpenGL ES 2.0 and Vulkan standards. As part of this task, it is requested to extend this library with new functionalities (like tracers), perform various benchmarking activities, and further extend the verification framework of the library.

Skills required: good programming skills, good knowledge of OS, basic knowledge of OpenGL standard

7. Developing and Extending the Shader Editor of the Company

The company is developing a set of tools for writing efficient code for the GPUs of the company. As part of this set of tools, a dedicated shader editor is being developed. As part of this project, the current shader editor of the company will be extended with new features and it will be ported to a new framework (e.g., Qt, eclipse, or a Python-based framework).
Skills required: C++ and Python Programming languages.

8. Extending the NemaGFX graphics API and GUI Builder tool with new Features

NemaGFX is a low level software graphics library developed by Think Silicon (http://think-silicon.com/products/software/nemagfx-api/). On top of NemaGFX, the company developed a new tool, called GUI Builder, that is able to design graphics applications in a drug-and-drop fashion and automatically generate code for Nema GPUs. As part of this project, it is requested to increase the efficiency of the generated code, to enhance the debugging capabilities of NemaGFX, and to extend the features of the GUI Builder.
Skills required: Very good background in C/C++ and graphics programming

9. Build the OpenVG API for Nema GPUs

OpenVG is a vector graphics processing API officially maintained by the Khronos group (https://www.khronos.org/). The purpose of this task is to port the OpenVG API to Nema GPUs of Think Silicon. This requires to fully understand the C code of OpenVG and write vertex and fragment shaders that will be accelerated in Nema GPUs.
Skills required: Very good background in C/C++ and graphics programming

10. Framework for On-Chip Debug Hardware

The purpose of this project is to build a framework for on-chip debug hardware (JTAG/UART etc). The framework will be applied to Nema GPUs and it should be able to insert HW breakpoints to monitor and visualize the current GPU execution state. Apart from the HW components, an additional SW utility component is needed to illustrate/visualize the GPU state in host PC.
Skills required: good knowledge HDL/Verilog.

11. Build Sample Games for NemaGFX Library

NemaGFX is a low level software graphics library developed by Think Silicon (http://think-silicon.com/products/software/nemagfx-api/). The purpose of this project is to develop simple and interactive games based on NemaGFX API.
Skills required: Very good background in C/C++ and graphics programming

12. Adaptive Management of Nema Display Controller based on Frame Rate

Nema display controller (Nema|DC) is a multi-layer display controller developed by Think Silicon. As part of this project, it is requested dynamically modify the generation of frames (output of Nema|DC)

and software calls when the application dictates a constant frame rate.
Skills required: OS background, basic knowledge of OS drivers and firmware.

13. Implementation of Backend for Qt-lite for Nema GPUs

Qt is a cross-platform application framework that is used for developing application software that can be run on various software and hardware platforms. In addition, Qt offers various features for developing graphics applications. As part of this task, it is requested to develop a backend for accelerating the Qt-based graphics applications in Nema GPUs.
Skills required: good programming skills, good knowledge of OS.

14. Port of Android Wear to Zynq SoC-based FPGAs

Android-Wear is a special version of Android OS customized for wearable devices. As part of this project, you are requested to port the Android-Wear in the Zynq (programmable logic + dual ARM processor as hard core) FPGA platforms.
Skills required: OS background, basic knowledge of OS drivers and firmware.

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